REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 102(b) Rejections

Examiner rejected claims 1-11 and 23-25 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,996,032 (hereinafter "Baker").

> To anticipate a claim, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Independent claims 1 and 23 include claim limitations that are not disclosed or suggested by Baker. In particular, applicant's independent claims include the claim limitation, or limitation similar thereto, of substantially simultaneously reading values from a plurality of registers, parsing a particular instruction, and determining a select number of registers to be modified in the plurality of registers, modifying a subset of the values in the select number of registers, and substantially simultaneously writing the values to the plurality of registers.

However, Baker does not disclose these limitations. The Examiner noted in the previous office action each bit in a multi-bit register addressable separately constitutes a separate single bit register. Applicant respectfully requests evidentiary support for Examiner's assertion. (MPEP ¶ 2144.03).

Rather, Baker discloses modifying different bits of the *same* register. (Baker, col. 3, lines 1-2). The reference further discloses writing data only to the predetermined bits

in a register write operation using a single write enable command. Accordingly, the method and system include writing to the predetermined bits using a single register write operation. (Baker, col. 3, lines 23-27). Thus, Baker fails to teach each and every element of the independent claims.

Furthermore, Baker teaches away from the claimed limitations. The reference discloses selected bits in a data register may be controlled without having to recall, specify, or operate on register bits not related to the particular bits of interest. (Baker, col. 3, lines 56-59). Baker further describes the ability to control register bits of interest without having to perform a read-modify-write operation. (Baker, col. 3. lines 3-7).

Accordingly, Baker does not anticipate independent claims 1 and 23. The remaining claims depend from one of the foregoing independent claims and thus include the novel claim limitations discussed above. Therefore, Baker does not anticipate claims 1-11 and 23-25.

Examiner rejected claims 1-11 and 23-25 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,991,531 (hereinafter "Song et al.").

> To anticipate a claim, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Independent claims 1 and 23 include claim limitations that are not disclosed or suggested by Song. In particular, applicant's independent claims include the claim limitation, or limitation similar thereto, of substantially simultaneously reading values from a plurality of registers, parsing a particular instruction, and determining a select number of registers to be modified in the plurality of registers, modifying a subset of the

values in the select number of registers, and substantially simultaneously writing the values to the plurality of registers.

However, Song does not disclose these limitations. The Examiner noted in the previous office action a vector register is equivalent to a plurality of registers. Applicant respectfully requests evidentiary support for Examiner's assertion. (MPEP ¶ 2144.03). Rather, Song discloses scalar registers are 32 bits wide and can contain one data element of any one of the defined sizes. The 256-bit vector registers support multiple data types as well as multiple elements. (Song, col. 4, lines 6-13). Moreover, the reference discloses each of the 32 bits in VGMR0 (or VGMR1) identifies an element to be operated on. Setting bit VGMR0 indicates that the element i of the vector register is to be affected, i being 0 to 31. (Song, col. 5, lines 43 – 50). Thus, Song fails to teach each and every element of the independent claims.

Accordingly, Song does not anticipate independent claims 1 and 23. The remaining claims depend from one of the foregoing independent claims and thus include the novel claim limitations discussed above. Therefore, Song does not anticipate claims 1-11 and 23-25.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned at (408) 720-8300, x329.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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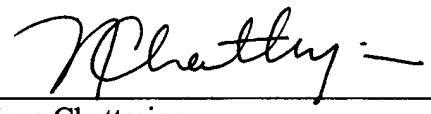

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